

Origin of the dielectric dead layer in nanoscale capacitors

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When the thickness of an oxide film is reduced to few unit cells, its dielectric properties (which are relevant, e.g., for nonvolatile ferroelectric memories and as gate oxides in MOSFET transistors) start to deviate from those predicted by macroscopic models, and cannot be disentangled from the metallic or semiconducting contacts. One particularly important issue related to interfacial effects is the “dielectric dead layer”, which plagues the performance of thin-film perovskite capacitors by substantially reducing the effective permittivity (κ) of the active high- κ material. The microscopic origins of this reduced permittivity, and in particular whether it stems from defects or from the fundamental properties of a metal/insulator interface, are not well understood.

To address this problem from first principles, we will first show how the macroscopic polarization (and the coupling to an external field) can be rigorously defined for a periodic metal-insulator heterostructure, by using techniques and ideas borrowed from Wannier-function theory. We will then demonstrate our new method by calculating the dielectric properties of realistic SrRuO₃/SrTiO₃/SrRuO₃ nanocapacitors. In particular, we demonstrate the existence of a dielectric dead layer and analyze its origin by extracting the ionic and electronic contributions to the electrostatic screening. We establish a correspondence between the dead layer and the hardening of the collective SrTiO₃ zone-center polar modes, and determine the influence of the electrode by repeating our calculations for Pt/SrTiO₃/Pt capacitors. Our results provide practical guidelines for minimizing the deleterious effects of the dielectric dead layer in nanoscale devices.